Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**ANODE**

**.015”**

**.015”**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .005” X .005”**

**Backside Potential: CATHODE**

**Process: D4**

**APPROVED BY: DK DIE SIZE .015” X .015” DATE: 9/23/21**

**MFG: FAIRCHILD THICKNESS .008” P/N: BAS16**

**DG 10.1.2**

#### Rev B, 7/19/02